SEMESTER EXAMINATION, APRIL-MAY, 2026

Course Name: -B.Tech(CSE) **Semester:- 4th**

Paper Name: -Computer Organisation and Architecture Paper Code:-NCS 404

Time - 3 Hrs + 20 minutes per hour extra time for V.I. & examinees with writer. Max Marks-70

Instructions:

- The question paper consists of three sections namely A, B, C. All sections are compulsory.
- Section A- Each question carries **3 mark**. **All questions are compulsory**.
- Section B- Answer any **5 out of 7** given questions. Each question carries **7 marks**.
- Section C- Answer any **2 out of 3** given questions. Each question carries **10 marks**.

Section – A
Multiple Choice Questions

1. Answer all the following questions. 5x3 =15

(i) Which register holds the address of the next instruction to be executed?

a) MAR
b) MDR
c) IR
d) Program counter(PC)

(ii) Convert -12.625 to binary

a) $(1100.101)_2$
b) $(-1100.101)_2$
c) $(-0110.011)_2$
d) $(-1101.010)_2$

(iii) Cache Coherency problem arises in:

a) Uniprocessor system
b) Pipelined system
c) Multiprocessor system
d) RISC processor

(iv) USB is an example of :

a) Processor
b) Memory
c) I/O interface
d) Cache

(v) Privileged instructions are executed in:

a) User mode
b) Interrupt mode
c) Kernel mode
d) DMA mode

Section – B
Short Answer Questions

2. Answer any five of the following questions. 5x7=35

i. Explain the functional block of a Computer, with proper diagram.

ii. What are the various Pipelining Hazards also mention the solution for those hazards.

iii. Differentiate between I/O programmed controlled transfer and DMA transfer, with a neat diagram.

iv. What is a Carry Look ahead adder? What are the drawbacks of Ripple adder?

v. Given, the Cache hit ratio is 0.9 , Cache access time is 100ns , and main memory access time is 1000ns. Calculate Average Memory Access Time (AMAT).

vi. What are cache coherence protocols? Also mention the cache write policies.

vii. Write short notes on :-

a) RISC & CISC

b) Software Interrupt & Exceptions

Section - C
Descriptive Questions

3. Answer any two of the following question. **2x10=20**

i) What do you mean by Memory Interleaving? What are the methods used for memory interleaving?

ii) Given page reference string:- 7,0,1,2,0,3,0,4,2,3,0,3,1,2,0. No. of frames = 3

Find the no. of page faults using: (a) Optimal (b) LRU

iii) What is a DMA Controller? Explain its working with a neat and labelled diagram.

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